Circuit Ideas

Digital sample and hold

To hold a sampled voltage for long periods, a process of digital approximation provides negligible drift. This circuit is t.t.l.-compatible and provides an analogue-to-digital conversion facility.

The basic element is an 8-bit binary counter using two cascaded 7493s. This provides 256 discrete voltage levels from the op-amp A_2. The input voltage provides a varying reference voltage to comparator A_1.

Applying a 0 at the reset input clears the counter for a period determined by the monostable. The counter now provides a staircase waveform, via A_2, to A_1. When the staircase is equal or greater than V_{in} the comparator goes high and disables the counter clock. The count is held and a sample voltage appears at the output. The reset state has to have a period greater than the sum of the monostable period and 256 clock periods. The speed of the clock is limited by the response of the op amps.

Greater accuracy may be obtained by cascading more counters, but at the risk of increasing the period between voltage transitions at the output. Digital conversion is available directly at the outputs of the counters.

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